AMENDMENTS TO CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

1 – 18. Canceled.

19. (Currently amended) An integrated electronic device comprising:

a semiconductor body having a substrate; ~~and~~

~~–~~a pair of ~~plurality of~~ insulation structures disposed in the substrate, delimiting an active area of the substrate, and each having a respective portions projecting from said substrate, the projecting portions defining a recess over a portion of the active area and over a portion of at least one of the insulation structures; and ~~wherein said insulation structures have respective recesses, which accommodate at least partially conductive regions~~

a memory cell having body region disposed in the portion of the active area, a floating gate disposed in the recess over the body region and over the portion of the at least one insulation structure, and a control gate disposed over the floating gate.

20. (Currently amended) The device according to claim 19 wherein:

said projecting portions define the recesses ~~are defined laterally with respect to respective projecting portions of said insulation structures~~ over respective portions of both of the insulation structures; and

said floating gate is disposed over the respective portions of both the insulating structures.

21. (Currently amended) The device according to claim 19 wherein said floating gate does not extend above the projecting portions of the insulating structures ~~conductive regions comprise terminals of memory cells arranged on top of respective said active areas and extending laterally inside at least one of said recesses~~.

22. (Currently amended) The device according to claim 19 wherein said floating gate does not extend laterally beyond the projecting portions of the insulating structures~~recesses are defined centrally with respect to respective said projecting portions of said insulation structures~~.

23. (Currently amended) The device according to claim 19~~22~~ wherein said floating gate has a surface facing the control gate, the entire surface being planar~~conductive regions are entirely accommodated inside respective said recesses~~.

24. – 25. Cancelled.

26. (Currently amended) An integrated circuit, comprising:

a substrate having an active region;

first and second insulators disposed adjacent to the active region and defining a recess over a portion of the active region~~ and over a portion of one of the insulators~~;

a body region of a memory cell disposed in the active region; and

a floating gate of the memory cell~~first conductor~~ disposed in the recess but not extending beyond the recess in a dimension parallel to a surface of the active region.

27. (Original) The integrated circuit of claim 26 wherein the first and second insulators respectively comprise first and second projections that define the recess.

28. (Original) The integrated circuit of claim 26, further comprising:

first and second trenches disposed in the substrate; and

wherein the first and second insulators are respectively disposed in the first and second trenches.

29. (Original) The integrated circuit of claim 26 wherein the first and second insulators define the recess over respective portions of both the first and second insulators.

30. (Currently amended) The integrated circuit of claim 26, further comprising a ~~third~~ gate insulator disposed between the floating gate~~first conductor~~ and the active region of the substrate.

31. (Currently amended) The integrated circuit of claim 26 wherein the floating gate does not extend above the first and second insulators~~active region and the conductor compose a memory cell~~.

32. (Currently amended) The integrated circuit of claim 26 wherein the first and second insulators define the recess over a portion of at least one of the first and second insulators~~the conductor composes a floating gate of a nonvolatile memory cell~~.

33. (Currently amended) The integrated circuit of claim 26, further comprising:

a gate~~third~~ insulator disposed on the floating gate~~first conductor~~; and
a control gate~~second conductor~~ disposed on the gate~~third~~ insulator and overlapping the floating gate~~first conductor~~.

34. (Currently amended) An integrated circuit, comprising:

a substrate;
a first isolation region~~insulator~~ disposed in the substrate and defining a recess that is bounded by the first isolation region on at least two sides; and
a first conductor disposed in the recess.

35. (Original) The integrated circuit of claim 34 wherein the first insulator comprises projections that define the recess.

36. (Original) The integrated circuit of claim 34, further comprising:

a trench disposed in the substrate; and
wherein the first insulator is disposed in the trench.

37. (Original) The integrated circuit of claim 34 wherein the first conductor composes a resistor.

38. (Original) The integrated circuit of claim 34 wherein the first conductor composes a plate of a capacitor.

39. (Original) The integrated circuit of claim 34, further comprising:

a second insulator disposed on the first conductor; and
a second conductor disposed on the second insulator and overlapping the first conductor.

40. – 48. Canceled.